



LESSON PLAN

Discipline: ETC	Semester: 5 th	Name Of The Teaching Faculty: SUGANDHA PUSPITA MADHUJHARA	
Subject: VLSI&ES (TH-2)	No. Of Days Per Week Class Allotted: 04 P	Semester From Date: 01.07.2024	To Date: 08.11.2024
		No. of weeks: 15	
Week	Class Day	Theory Topic	
1 st week	1 st	➤ Introduction to VLSI	
	2 nd	➤ Classification of CMOS digital circuits	
	3 rd	➤ Introduction to MOS transistor, structure	
	4 th	➤ Basic operation of MOS	
2 nd week	1 st	➤ MOS I-V characteristics	
	2 nd	➤ MOS capacitance	
	3 rd	➤ Modelling of MOS	
	4 th	➤ Flow of circuit design procedure	
3 rd week	1 st	➤ Y-chart	
	2 nd	➤ Design hierarchy	
	3 rd	➤ VLSI design style-FPGA, gate array design, Standard cell-based design, full custom design	
	4 th	➤ Fabrication of MOSFET, Basic steps of fabrication	
4 th week	1 st	➤ Fabrication of nMOS	
	2 nd	➤ Fabrication of pMOS	
	3 rd	➤ Some important terms related to fabrication	
	4 th	➤ MOS fabrication process by n-well on p-substrate	
5 th week	1 st	➤ MOS fabrication process by n-well on p-substrate	
	2 nd	➤ MOS fabrication process by p-well on n-substrate	
	3 rd	➤ MOS fabrication process by p-well on n-substrate	
	4 th	➤ Layout design rule	
6 th week	1 st	➤ Stick diagram	
	2 nd	➤ nMOS inverter	
	3 rd	➤ VTC of nMOS inverter	
	4 th	➤ Resistive load nMOS inverter	
7 th week	1 st	➤ Inverter with MOSFET load	
	2 nd	➤ Inverter with MOSFET load	
	3 rd	➤ CMOS inverter	
	4 th	➤ CMOS inverter	
8 th week	1 st	➤ Delay time definitions	
	2 nd	➤ Inverter with delay constraints	
	3 rd	➤ Static combinational digital logic design	
	4 th	➤ 2 i/p CMOS NAND gate	
9 th week	1 st	➤ Layout of simple CMOS logic gates	
	2 nd	➤ Complex logic circuits	
	3 rd	➤ CMOS transmission gate	
	4 th	➤ Sequential MOS logic circuits	
10 th week	1 st	➤ S-R latch circuit	
	2 nd	➤ Clocked S-R latch	
	3 rd	➤ Dynamic logic circuits	
	4 th	➤ Dynamic pass transistor circuits	
11 th week	1 st	➤ Semiconductor memories, DRAM	
	2 nd	➤ DRAM	
	3 rd	➤ SRAM, Flash memory	
	4 th	➤ Design Language (SPL & HDL) & HDL	

